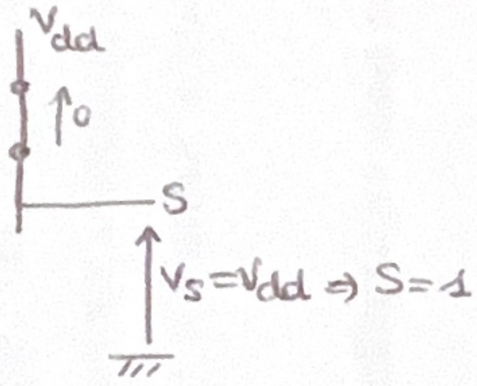
Circuits avec interrupteurs commandés pour les 4 portes logiques

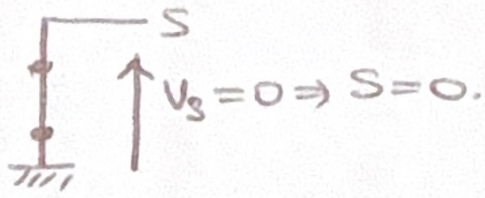
ChE3

a) une entrée E

si E = 0



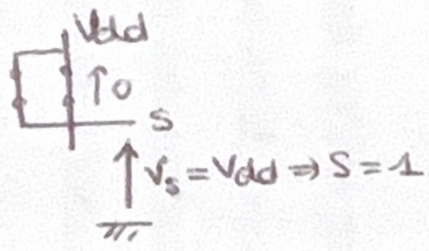
si E = 1



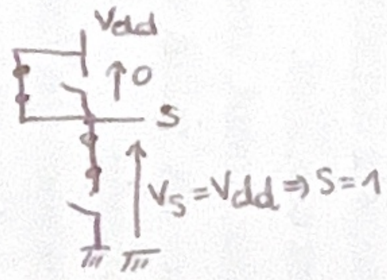
CCL : porte NOT

b) deux entrées A et B

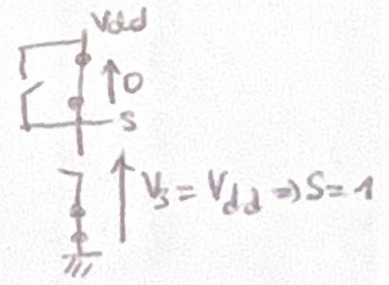
si A = 0 = B



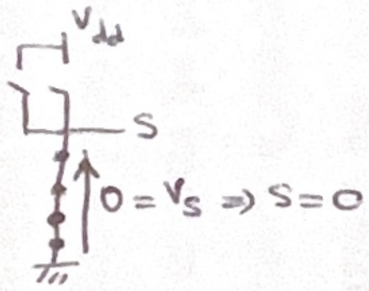
si A = 0
B = 1



si A = 1
B = 0



si A = 1 = B

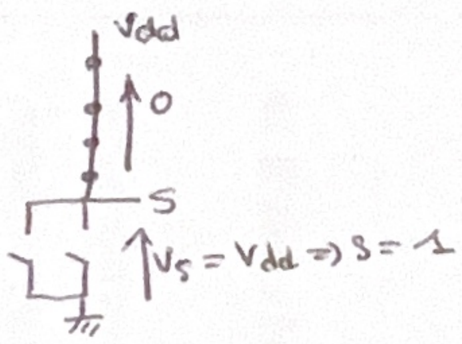


A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

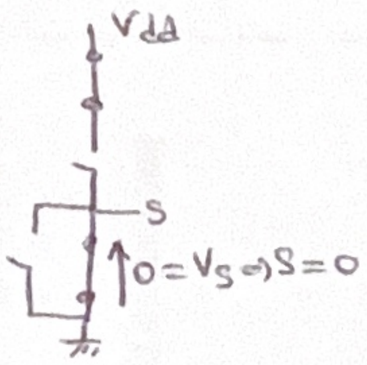
CCL : porte NAND

c) deux entrées A et B

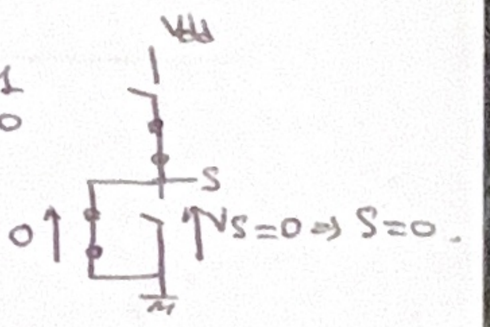
si A = 0 = B



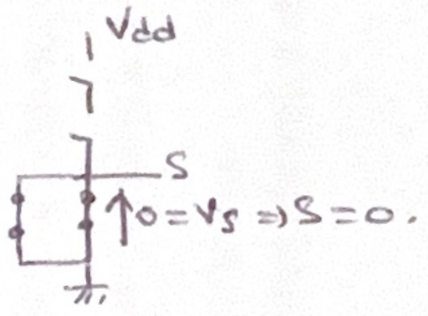
si A = 0
B = 1



si A = 1
B = 0



si A = 1 = B

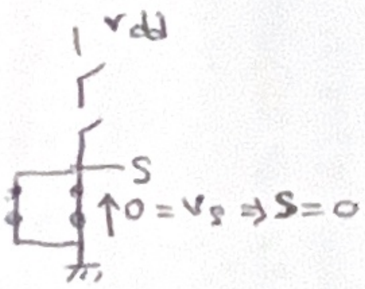


A	B	S
0	0	1
0	1	0
1	0	0
1	1	0

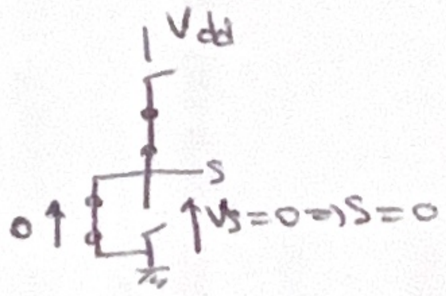
CCL : porte NOR

d) deux entrées A et B.

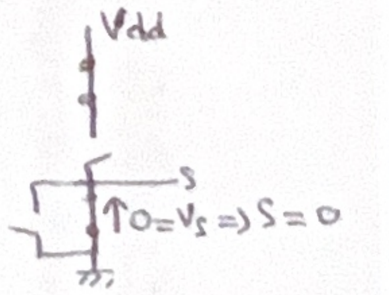
si A = 0 = B



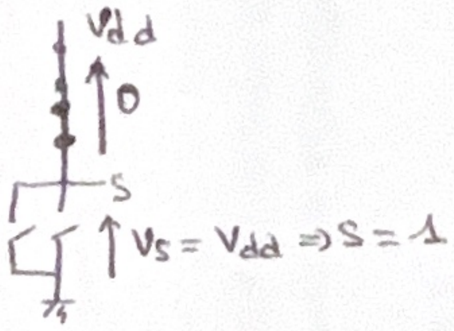
si A = 0
B = 1



si A = 1
B = 0



si A = 1 = B

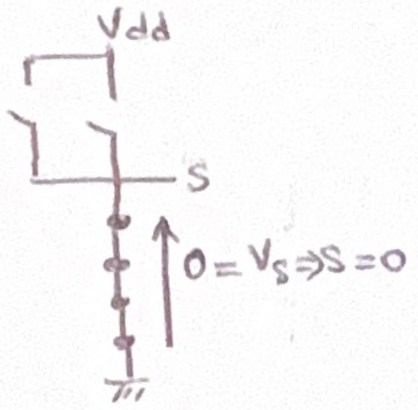


A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

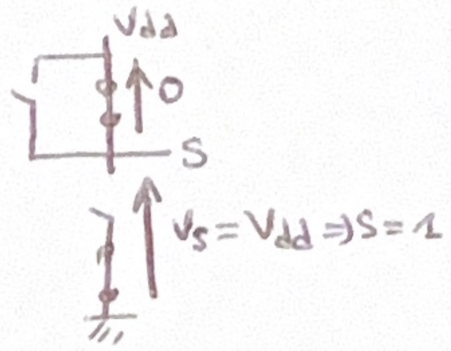
CCL : porte AND

e) deux entrées A et B

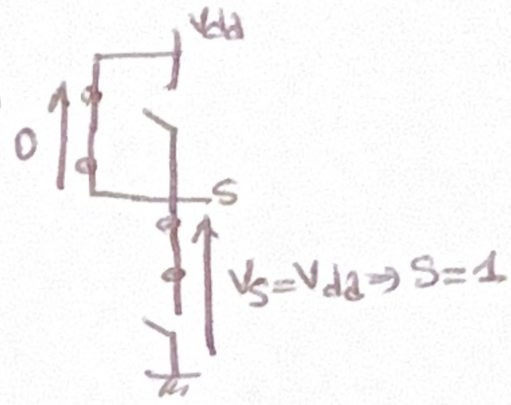
si A=0=B



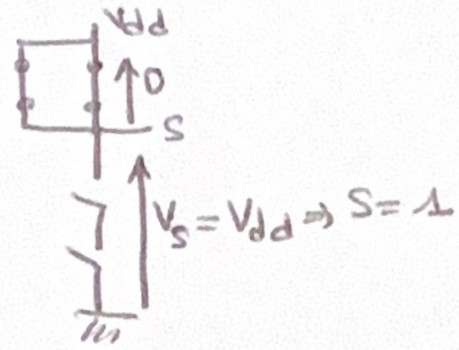
si A=0
B=1



si A=1
B=0



si A=1=B



A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

CCL : porte OR